REPORT DOCUMENTATION PAGE

Form Approved
OMB NO. 0704-0188

1. AGENCY USE ONLY (Leave Blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	12/20/00	Final Report: 9/25/98 - 9/24/00

4. TITLE AND SUBTITLE
Large Scale Systems Development Using the MacroMosaics Concept

5. FUNDING NUMBERS
DAAG55-98-1-0525

6. AUTHOR(S)
Mahdi Abdelguerfi and Ming-Cheng Cheng

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
University of New Orleans, Lakefront
New Orleans, LA 70148

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
U. S. Army Research Office
P.O. Box 12211
Research Triangle Park, NC 27709-2211

10. SPONSORING / MONITORING AGENCY REPORT NUMBER
ARO 39656.4-EL

11. SUPPLEMENTARY NOTES
The views, opinions and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy or decision, unless so designated by other documentation.

12 a. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12 b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

This project is to perform a preliminary study of the MacroMosaics technology and to establish a framework for a suite of IC CAD tools from Mentor Graphic Corporation necessary for implementation of VLSI/ULSI integrated circuit design and the MacroMosaics architecture at University of New Orleans. To utilizing the CAD tools more efficiently, the PI has attended some training courses for the CAD tools. Based on our study and on the interactions with Clear Logic and HiDEC, it is believed that the MacroMosaics architecture combined with SHOCC interposer technology will offer both commercial and military designers flexibility to use on-chip resources more efficiently. The MacroMosaics technology will lead to lower cost, higher performance, and more energy-efficient design methodology for large-scale electronic systems.

The MacroMosaics is a predefined architecture consisting of a library of IC building blocks combined with SHOCC (Seamless High Off-Chip Connectivity) interposer technology. We have selected the next generation CMOS based on the Silicon-On-Insulator (SOI) technology as one of the building-block sets for this project with emphasis on low power applications. The SOI CMOS device structure has been designed and studied to achieve low-power and high-speed performance. Layout verification and Circuit level-simulation for the inverters and other building blocks and will be carried out in the established suite in the near future.

14. SUBJECT TERMS	15. NUMBER OF PAGES
MicroMosaics, building blocks, SOI, low power, integrated circuits	3
	16. PRICE CODE

17. SECURITY CLASSIFICATION OR REPORT	18. SECURITY CLASSIFICATION ON THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

NSN 7540-01-280-5500
(Rev.2-89)
Prescribed by ANSI Std. 239-18

Standard Form 298

298-102

Final Progress Report

1. Statement of work

The objective of this project is to perform a preliminary study of the MacroMosaics technology and to establish a framework for a suite of integrated-circuits CAD tools for implementation of the MacroMosaics architecture and VLSI/ULSI integrated circuit design and at University of New Orleans (UNO). The MacroMosaics is a predefined architecture consisting of a library of silicon IC building blocks, interconnected by means of a high density SHOCC (Seamless High Off-Chip Connectivity) [1,2] interposer. The work that has been performed in this project also includes, although not required, the study of the building blocks that will eventually be used to construct the MacroMosaics architecture and will be implemented in the established suite for low power applications.

2. Summary of the important results

(1) The IC CAD suite from Mentor Graphics Corporation has been established at UNO. This will allow us to carry out further studies of the MacroMosaics architecture combined with the SHOCC interposer technology and other microelectronics approaches to improve performance of large-scale electronic systems.

(2) The established suite will provide a complete set of IC design tools for faculty in the Computer Science Department and the Electrical Engineering Department at UNO to improve their microelectronics and VLSI curricula and research capabilities.

(3) Low-power building blocks with high-speed performance are selected in the project for preparation of implementing the MacroMosaics technology in the established suite. An MOS device structure based on the SOI (Silicon-On-Insulator) technology has been proposed to optimize both high-speed and low-power performance. The proposed SOI devices utilize the conventional dynamic-threshold concept [3,4] for low-threshold design to improve low-power performance but use an unconventional inhomogeneous body structure to enhance the body effect [5-7]. This unconventional structure improves the static power and further increases the driving capability for higher speed performance [7].

3. List of publications resulting from support of the project

- Jun Xu and Ming-C. Cheng, "Investigation of Dynamic-Voltage SOI MOSFET's with Low-Impurity-Density Channels", *Proc. of 1999 International Semiconductor Device Research Symposium,* pp. 93-93, Charlottesville, Virginia, Dec, 1-3, 1999.
- Jun Xu and Ming-C. Cheng, "Design Optimization of High Performance Low Temperature MOSFET's with Low-Impurity-Density Channel below 1 Volt," *IEEE Trans. Electron Devices*, vol. 47, pp. 813-821, April, 2000.
- Jun Xu and Ming-C. Cheng, "A Dynamic Threshold-Voltage SOI MOSFET with a Stepped Channel Doping Profile", *Proc. of the Third IEEE International Caracas Con. on Devices, circuits, and Systems*, pp. D29.1-D29.5, Cancun, Mexican, March 15-17, 2000.
- Ming-C. Cheng and Jun Xu, "Influence and Improvement of the Body Effect on Performance of Dynamic Threshold MOSFETs at Low Supply Voltages", prepared for publication.

4. List of all participating scientific personnel

- **Principal Investigator:** Mahdi Abdelguerfi, Dept. of Computer Science, University of New Orleans, New Orleans, LA 70148; Email: mahdi@cs.uno.edu
- **Co- Principal Investigator:** Ming-Cheng Cheng, currently in Dept. of Electrical & Computer Engineering, Box 5720, Clarkson University, Potsdam, NY 13699; Email: mcheng@clarkson.edu
- **Post-Doctor Researcher:** Jun Xu, supported during Dec 1998 – October 1999, currently in Microelectronics Institute, Tsinghua University, Beijing, China
- **Graduate Students:**
  - Haider Mohamed Sharif, Ph.D. student in Computer Science at University of New Orleans.
  - Wai-Kay Yip, expected to receive his Ph.D. degree in Electrical Engineering in December 2001 from University of New Orleans

5. Bibliography

[1] M. Dibbs, P. Garrou, C.C. Chau, et al., "Development of Seamless High Off-Chip Connectivity," pp. 138-143, International Symposium on Microelectronics, 1997.

[2] S. Afonso, L. W. Schaper, H. A. Naseem, "Modeling and Electrical Analysis of Seamless High Off-Chip Connectivity (SHOCC) Interconnects," IEEE Tran. Advanced packaging, Vol. 22, 309 (1999)

[3] F. Assaderaghi, D. Sinitsky, S. A. Parke, et al., "Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI," IEEE Trans. Electron Devices, 44, p. 414 (1997).

[4] J. P. Colinge, "An SOI Voltage-Controlled Bipolar-MOS Device," IEEE Trans. Electron Dev, 34, p. 845 (1987).

[5] Jun Xu and Ming-C. Cheng, "Investigation of Dynamic-Voltage SOI MOSFET's with Low-Impurity-Density Channels", *Proc. of 1999 International Semiconductor Device Research Symposium,* pp. 93-93, Charlottesville, Virginia, Dec, 1-3, 1999.

[6] Jun Xu and Ming-C. Cheng, "A Dynamic Threshold-Voltage SOI MOSFET with a Stepped Channel Doping Profile", *Proc. of the Third IEEE International Caracas Con. on Devices, circuits, and Systems*, pp. D29.1-D29.5, Cancun, Mexican, March 15-17, 2000.

[7] Ming-C. Cheng and Jun Xu, "Influence and Improvement of the Body Effect on Performance of Dynamic Threshold MOSFETs at Low Supply Voltages", prepared for publication.